PC Interfacing

Fourth Level

Lecture Four

Experiment board design and Expanding the Centronic

Goals:
Up-on completing this lecture, the student should be able to:

1- Build ccts to enable the safe interfacing with the parallel port.
2- understand the current limitations of the output.
3- Understand how to use the octal buffer

1. Centronic experimental board:-

Figure 2.18 shows the circuit diagram of the Centronic experimental board. DB0 to DB7 of the data port of the Centronic port are fed into the inputs of 74LS244 Schmitt trigger buffers (IC2) via eight 100 Ω resistors (RL2, eight-way resistor array). The outputs of the buffers are connected to an eight-way detachable screw terminal. Each line is also connected to a low current LED via a 3.3K resistor.

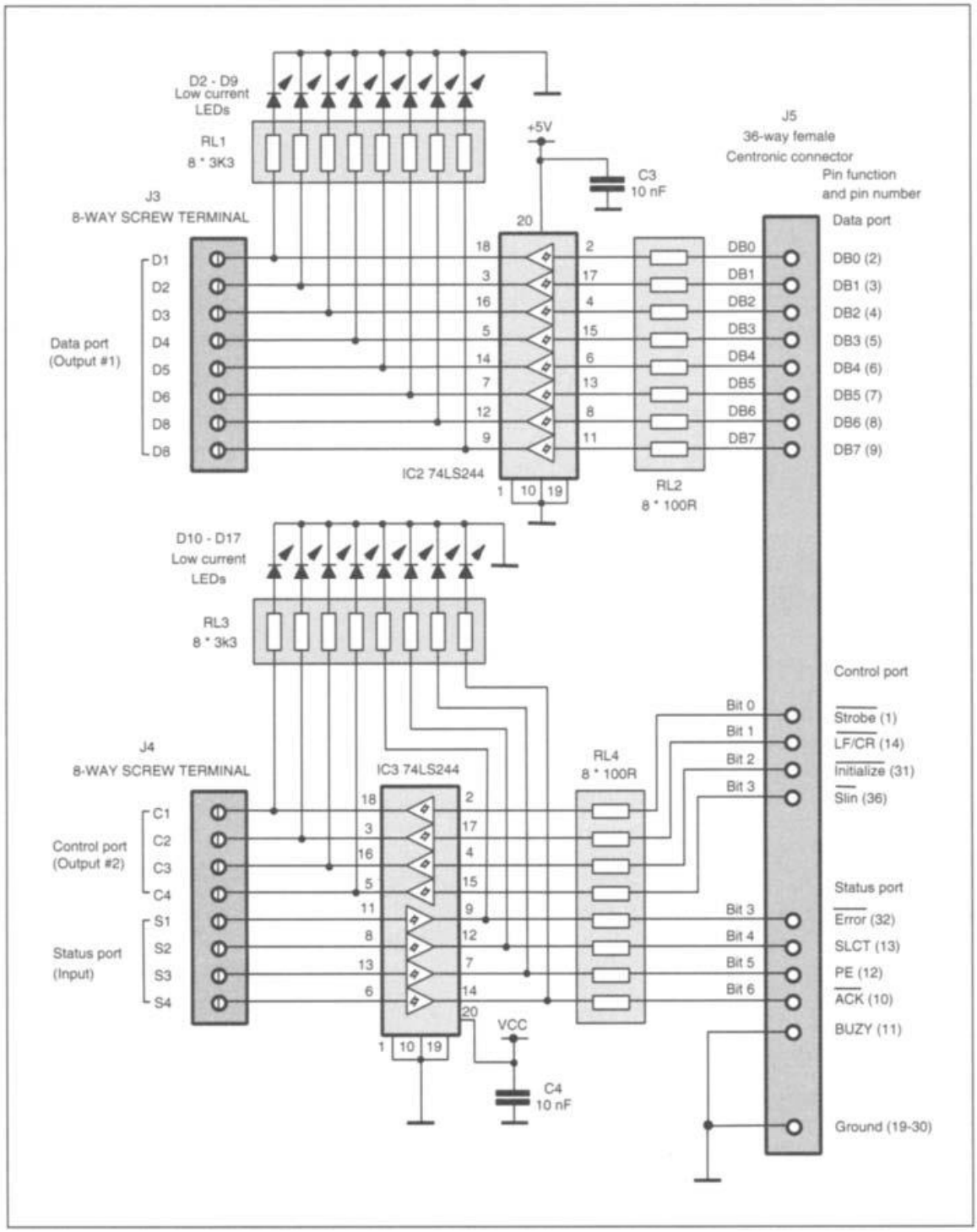

Fig. 2.18: Circuit of the Centronic experimental board

When a line has a logic high state, the corresponding LED illuminates. The four output lines of the control port are connected in the same way as for the data port. Four inputs are connected to the inputs of four Schmitt trigger buffers of IC3. The outputs of the buffers are connected to the four input lines of the status port via four 100Ω resistors. The status port has five input lines, but only four of them are connected this way. The logic status of these lines is monitored by LEDs.

The fifth input line of the status port (the BUZY input) is connected permanently to the ground. This is a very useful feature if high level printer control commands are used to control the board. This indicates that the Centronic experimental board is always ready to receive data.

The power supply incorporates a 1A +5V 7805 fixed voltage regulator (see Figure 2.19). Power is fed to the board via a power connector SK1. SW1 controls the on/off of the power. A 1A fuse is used on the board to limit the total current. The on/off status is indicated by an LED. The input unregulated power supply and the regulated +5V DC are both connected to a four-way screw terminal (J1). The components utilized on the board are listed in Table 2.1.

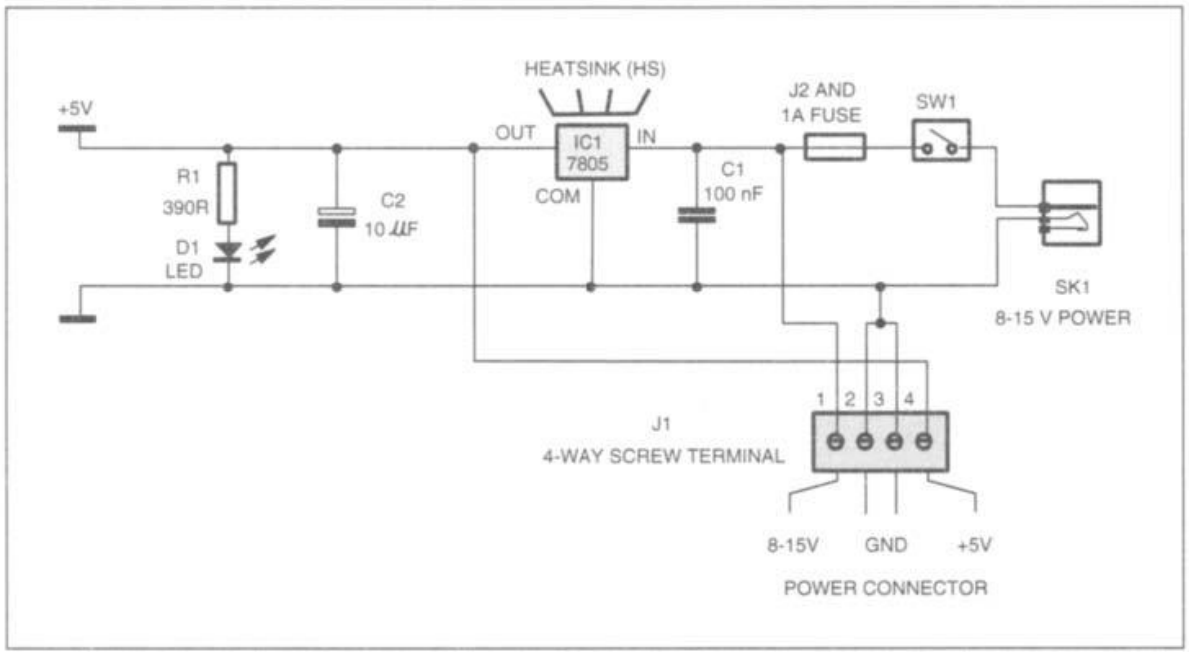

Fig. 2.19: Power Supply Circuit for the three interfacing boards

Table 2.1

Resistors (all 1% 0.25W metal film resistors)	
R1	390R
RL1, RL3	3.3K eight-way resistor array
RL2, RL4	100R eight-way resistor array
Capacitors	
C1, C3, C4	100 nF
C2	10 µF
Semiconductors	
IC1	7805 1A +5V voltage regulator
IC2, IC3	74LS244
D1	5mm green LED
D2–D17	Low power 3 mm red LEDs
Connectors	
J1	Four-way detachable screw terminal block set
J2	Fuse holder
J3, J4	Eight-way detachable screw terminal block set
J5	36-way female Centronic type connector
SK1	2.5 mm male power connector
Others	
SW1	PCB mounting miniature SPDT switch
Fuse	1A 25 mm length
Heat sink	(5 deg/watts)
PCB boards	
Holders for 3mm LEDs	
PCB pilar & screws	

In many applications, the number of I/O lines provided by the Centronic, RS232 and game port is not enough. Expansion of the I/O lines is required.

2. Expanding the Centronic port:

One method for expanding I/O lines of the port is to use the 74LS TTL or 4000 CMOS series logic chips. The other is to use dedicated peripheral programmable interface (PPI) chips such as the 8255, 8155 or others. Using the logic chips is simple and economical. The disadvantage is that the hardware is not configurable. Using interface chips makes the expansion configurable. For example, the 8255 PPI provides 24 I/O lines which are arranged in three groups, A, B and C. Each group has eight I/O lines and can be configured as an input or an output port.

(a) Reading 8- bits data:

Figure 4.1 shows an experimental circuit to allow the Centronic port to read 8-bit data using a 74LS241 octal buffer. The pin-out of the 74LS241 is shown in Figure 4.1. When pin 1 is taken low, the four buffers on the left hand side are enabled (the outputs follow the inputs). Otherwise the outputs are in the high the impedance state. When pin 19 goes high the four buffers on the right hand side are enabled. If pins 1 and 19 are connected together to form a data selection line (DSL), by putting it low and then high, you can read the four bits connected to the buffers on the left and then the other four bits connected to the buffers on the right in turns. Operating in such a manner, 8-bit data can be read into the computer via only four lines. The DSL line can be controlled by bit 0 of the data port.

Octal buffer used to read 4 bits and other 4 bits are in high impedance state. The DSL line connected to the both low and high signal to read 4 bits lower data and 4 bits upper data in turns via four data lines. The DSL can be controlled by D0 line to read byte data in two consecutive readings.

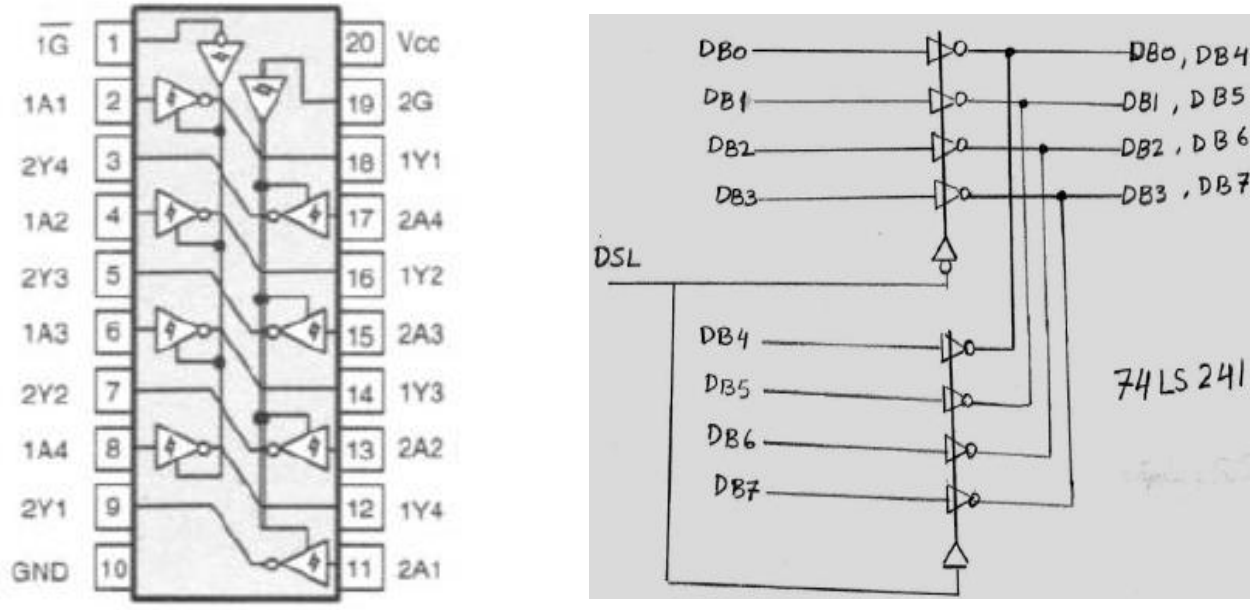

Fig. 4.1: The pin-out of the 74LS241

Figure 4.1 also shows how the 74LS241 is connected to the Centronic experimental board. Eight-bit input data is loaded into a computer in two consecutive

readings. When SEL is low, bit 0 to bit 3 of the input data are read into the computer. When SEL is high, bit 4 to bit 7 are read into the computer.

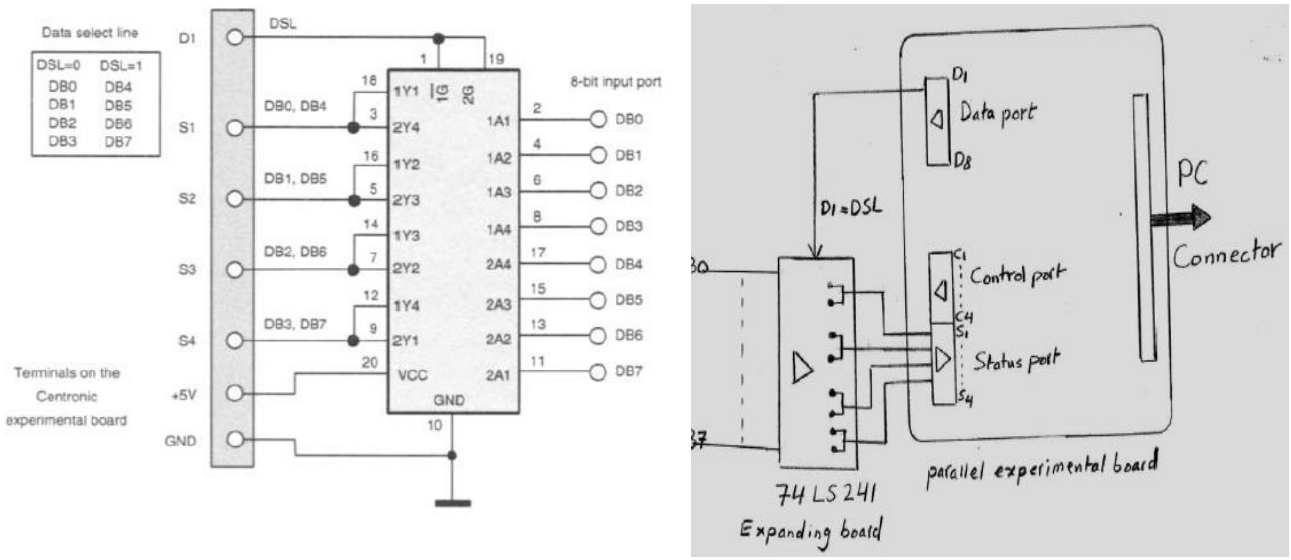

Fig. 4.1: The connection between 74LS241 and the Centronic experimental board.

(b) Expanding Outputs:

The way to expand output lines are to use latches such as the 74LS373 or 74LS374 ICs. The pin-out and an experimental circuit using the 74LS374 are shown in Figure 4.2. The inputs to the 74LS374 are connected to bit 0 to bit 7 of the DATA port. Latching data into the IC is controlled by the CLK. The CLK pin is controlled by one output line of the CONTROL port. In Figure 4.2, D1 to D8 and C1 are terminals on the Centronic experimental board.

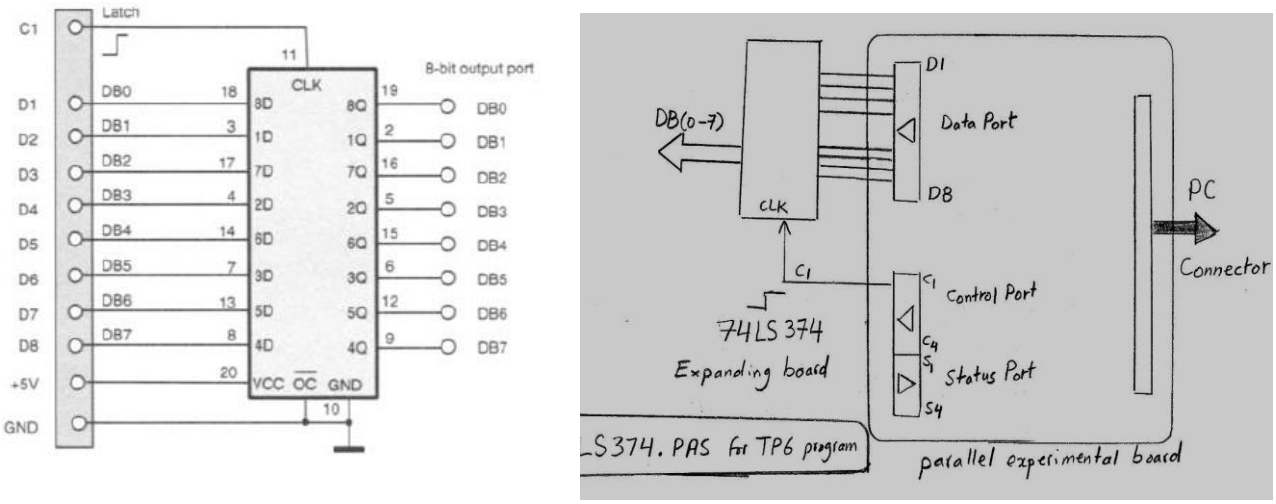

Fig. 4.2: connection between 74LS374 and the Centronic experimental board

(c) I/0 expansion using 8255 PPI chips:

Use Peripheral programmable interface (PPI) chip, such as 8255, 8155 or others. The expansion configurable 8255 provides 24 I/O Lines arranged in 3 groups A, B, and C. Each group has 8 I/O Lines and can be configured as input or output port.

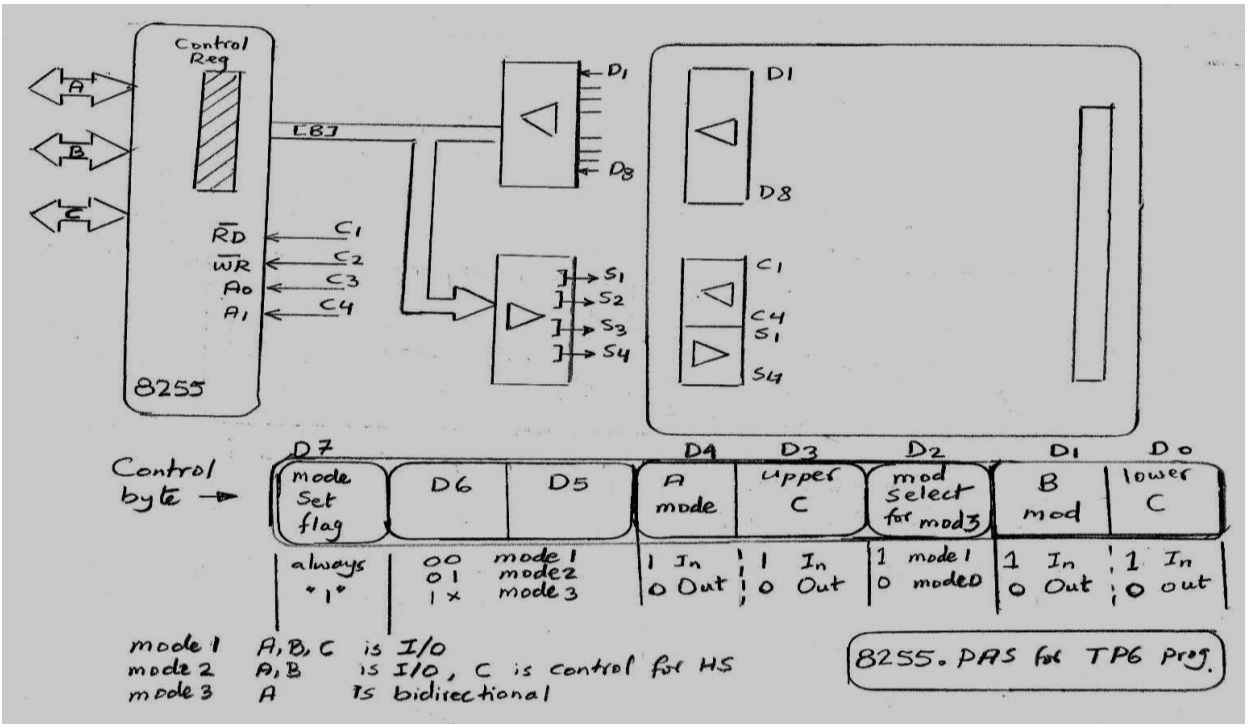

Fig. 4.3: connection between 8255 and the Centronic experimental board

The 8255 has three operation modes:

- In Mode 1, the ports A can be configured as an 8-bit input or output port. Mixture of inputs and outputs is not possible. Port B is the same as port A. Port C is split into two halves (the upper four bits and lower four bits). Each half can be configured as either input or output. The mixture of inputs and outputs within each half is not possible.
- In Mode 2 configures the 8255 PPI as strobed I/O ports. Ports A and B are configured as two independent 8-bit input or output ports. Each of them has a 4-bit control port associated with it. The control ports are formed by the lower and upper four bits of port C, respectively.
- In Mode 3, port A can be configured as a bidirectional port. Port B is in Mode 0 or Mode 1.

The modes of the 8255 are configured by writing an 8-bit control word to the control register. The bit function of this control word is shown below:

bit 7 (mode set flag) always 1

bit 6, Bit 5 (mode selection bits) 00=Mode 1, 01=Mode 2, lx=Mode 3

bit 4 (mode of port A) 1=input, 0=output

bit 3 (mode of upper half of C) 1=input, 0-output

bit 2 (mode selection for Mode 3) 1-Mode 1, 0-Mode 0

bit 1 (Mode of port B) 1=input, 0=output

bit 0 (Mode of lower half of C) l=input, 0-output

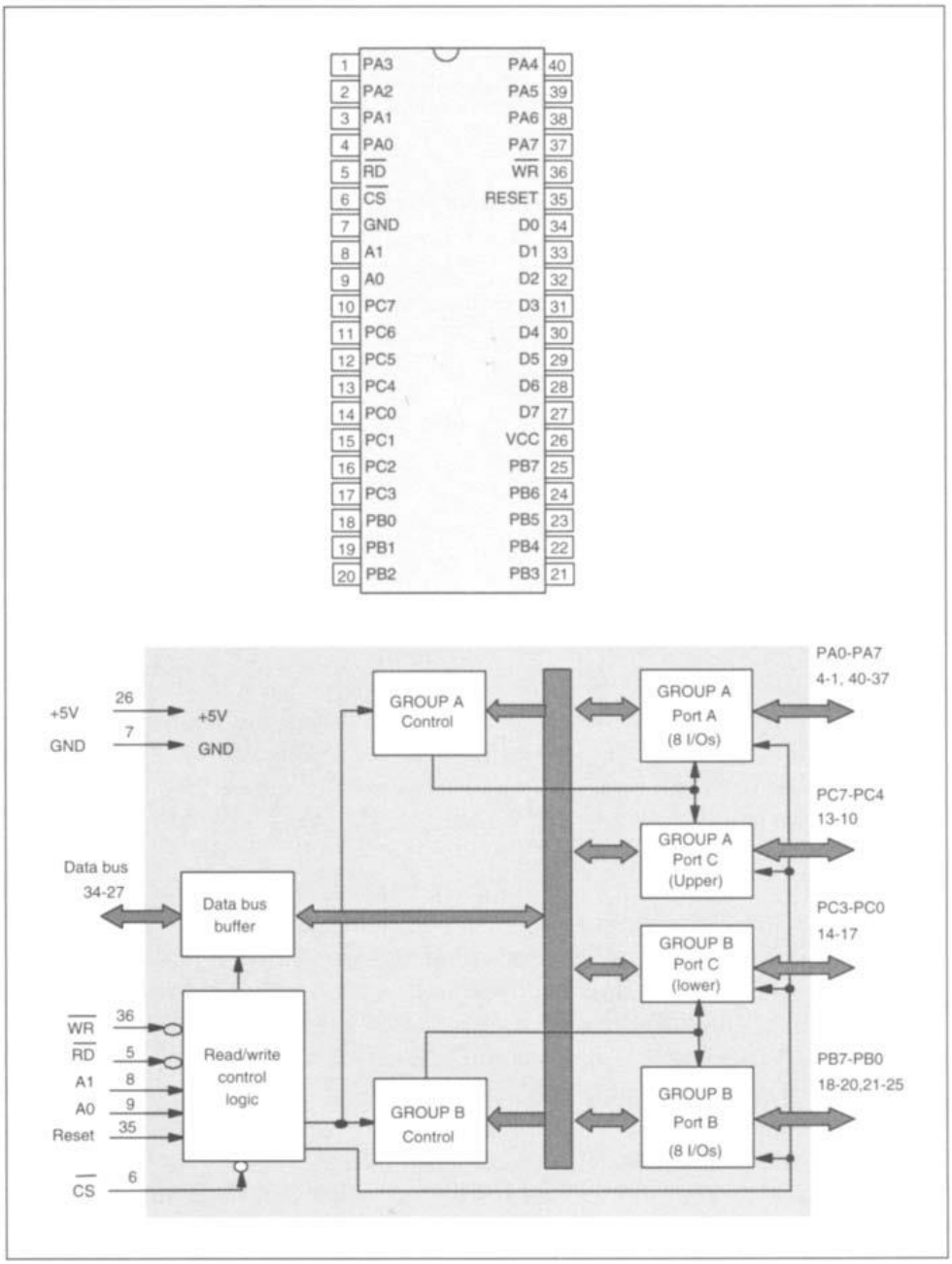

Fig. 4.4: pin out and internal block diagram of the 8255

Summary:

1- octal buffers hugly increase the capabilities of the parallel ports.

2- current limiting resistors and schmitt-triggers provide output protection and driving capabilities.

Questions:

1- Design a circuit to connect four 8-bit A/D devices to the parallel port, write the pseudo code as well.

2- How does the tri-state buffer works?