PC Interfacing

Fourth Level

Lecture Five

Experiment board design and Expanding the RS232

Goals:
Up-on completing this lecture, the student should be able to:
1- Build interfacing circuits to protect and drive the serial port.
2- Comprehend the concept of Line-drivers
3- Comprehend the concept of UART Programmable Chips.

1. Serial RS232 experimental board:-

The circuit diagram of the RS232 experimental board is given in Figure 2.20. The three outputs of the RS232 port of a PC (TD, RTS and DTR) are fed into the MAX238 RS232-TTL driver/receiver (IC3, Maxim), where the RS232 voltage level is converted to TTL level. The outputs from the IC3 are fed into Schmitt trigger buffers 74LS244 (IC2), the outputs from which are connected to three screw terminals (J3). The logic status of each line is monitored by low current LEDs. The four input signals (RD, DSR, DCD and CTS) are fed into the 74LS244 buffers. The outputs from the buffer are fed into IC3 where the TTL voltage level is converted into the RS232 level. Their logic status is monitored by LEDs. The power supply system is the same as that for the Centronic experimental board. The MAX238 is an RS232/TTL receiver/transmitter; it's requiring only a single +5V supply. The two on-chip charge pump voltage converters generate +10 V and -10 V power supplies from a single +5 V supply. The IC contains eight voltage level converters, four of which convert the TTL/CMOS level into the RS232 level, and four of which convert the RS232 voltage level into the TTL/CMOS level. It requires five external 1µF capacitors. The components utilized on the board are listed in Table 2.2.

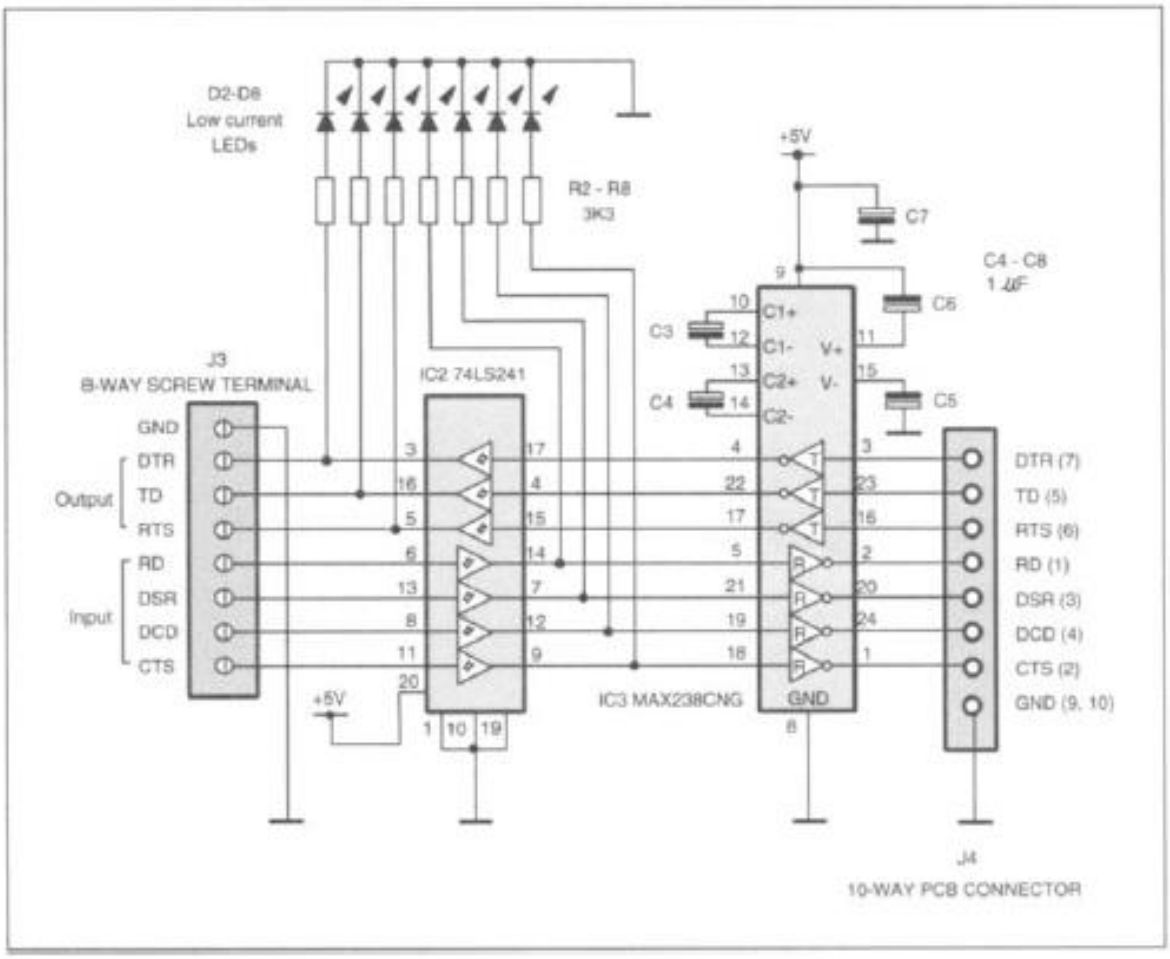


Figure 2.20 Circuit diagram of the RS232 experimental board

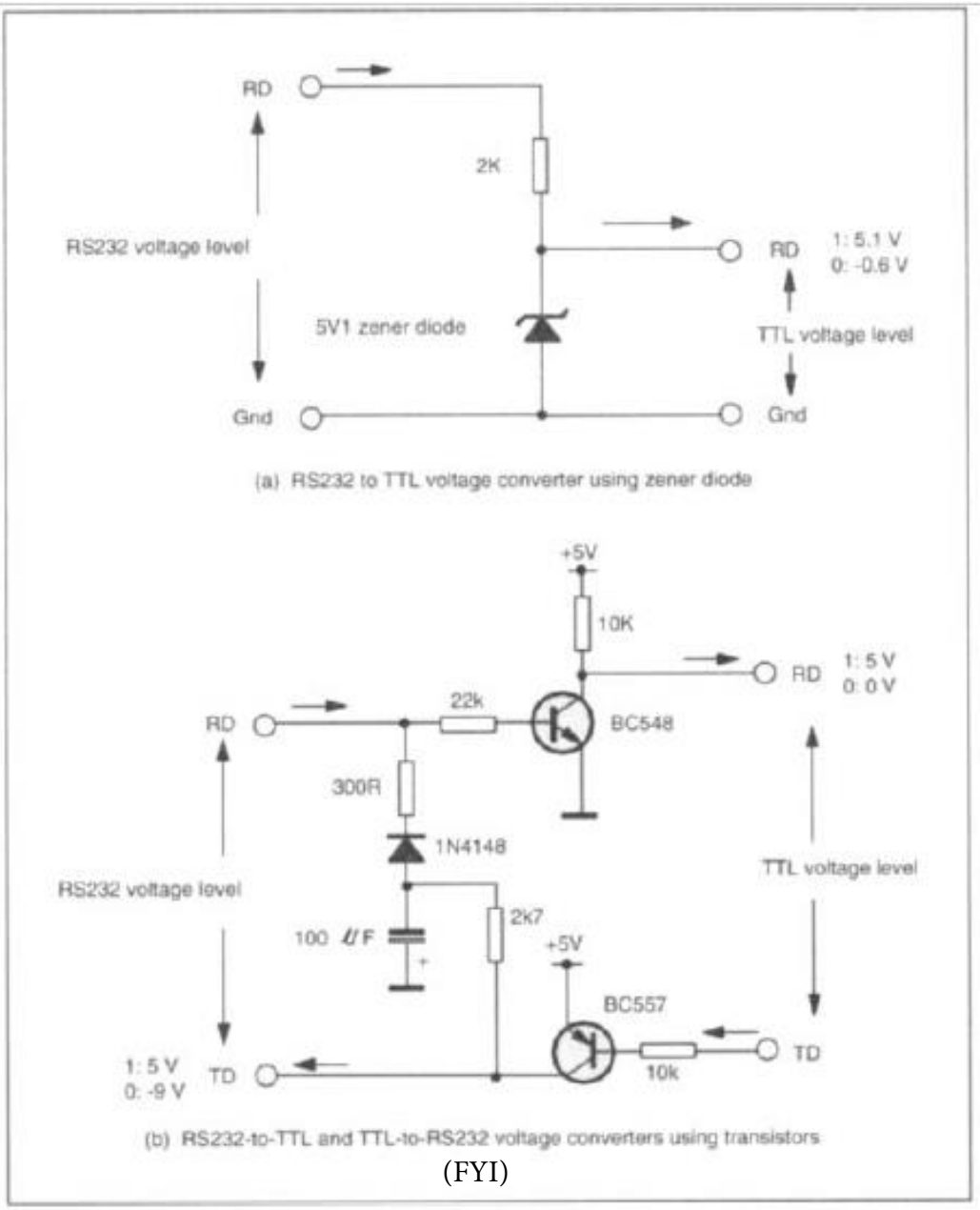
Table 2.2

Resistors (all 1% 0.25W metal film resistors)	
R1	390R
R2-R8	3.3K
Capacitors	
C1	100 nF
C2	10 µF
C3-C7	1 µF
Semiconductors	
IC1	7805 1A +5V voltage regulator
IC2	74LS244
IC3	MAX238CNG
D1	5mm green LED
D2-D8	Low power 3mm red LEDs
Connectors	
J1	Four-way detachable screw terminal block set
J2	Fuse holder
J3	Eight-way detachable screw terminal block set
J4	Ten-way PCB connector set
SK1	2.5mm male power connector
Others	
SW1	PCB mounting miniature SPDT switch
Fuse	1A 25mm length
Heat sink	(5 deg/watts)
PCB boards	
Holders for 3mm LEDs	
PCB pilar & screws	
9 pin female D-type connector and housing	
1m 9 core digital signal cable	

2. RS232/TTL line translators:

The simplest way of converting the RS232 voltage level to the TTL voltage level is to use **voltage clamp** circuits as shown in Figure 4.5(a). The circuit consists of one resistor and a +5.1V Zener diode. When the input RS232 status is high, the output is +5 V when the status is low, the output voltage is -0.6V. **Another TTL/RS232** transceiver circuit is shown in Figure 4.5(b). The circuit does not require any external power supplies. It 'steals' the power from the RS232 port. It has an inverting action.

The TTL/RS232 transceivers ICs are widely used. The MAX232 and the MAX238 are two examples. Both ICs require a signal rail +5V power supply. The MAX232 contains an on-board dual charge-pump DC-DC voltage converter, two RS232 drivers and two RS232 receivers. The dual charge-pumps convert the +5 V supply voltage to +10V and -10V. Care should be taken not to load V+ and V- to a point that it violates the minimum RS232 (RS232C, V_{min} = 3V) voltage level. The supply current of the MAX232 is 4 mA when the outputs have no load. The MAX238 has similar electrical characteristics and has four drivers and four receivers.



(FYI)

Figure 4.5 TTL/RS232 voltage converter circuits

3. Expanding the RS232 port (using UARTs):-

The CDP6402 is a Universal Asynchronous Receiver/Transmitter for interfacing to asynchronous serial data channels. Serial data format is programmable. It can have 5, 6, 7, or 8 bit length. The parity check can be odd, even or none. Stop bits can be 1, 1.5 or 2. The IC requires a power supply voltage 4 to 10 volts. The pin-out and the internal block diagram are shown in Figure 4.8. Pin 21 is the Master Reset (MR), which should be at the logic low state in normal operations. Pins 35 through 39 control the serial data format. To enable the control pins, pin 34 (Control Register Load, CRL) must be at logic high. A high level on pin 35 (Parity Inhibit, PI) inhibits parity generation and check. It also forces the Parity Error (PE, pin 13) pin to stay low. When PI is low, a high level on Even Parity Enable (EPE, pin 39) selects even parity. A low level on EPE pin selects odd parity. Pin 36 (Stop Bit Select) high selects 1.5 stop bits for 5 character format and 2 stop bits for other data lengths. If it is low, 1 stop bit is selected. Pins 37 (Character Length Selected, CLS2) and 38 (CLS1) select the data length: CLS1=0, CLS2=0 for 5 bits; CLS1=1, CLS2=0 for 6; CLS1=0, CLS2=1 for 7 and CLS1=1 and CLS2=1 for 8.

Pins 17 (Receiver Register Clock) and 40 (Transmitter Register Clock) are the clock inputs for the receiver and transmitter. They are normally connected together. Pin 20 (Receiver Register Input, RRI) is the serial data input. The received data is stored in the receiver buffer registers which are accessed via pins 5 to 12 (Receiver Buffer Registers). Pin 4 (Receiver Register Disable, RRD) should be low. When data is successfully received and loaded into the receiver buffer registers, pin 19 (Data Received) goes from low to high. It can be set to low by making pin 18 (-Data Received Reset) low. Pins 13 (Parity Error), 14 (Framing Error) 15 (Overrun Error) give the status of errors occurring during a data transmission and they are all high active. To enable these status outputs, pin 16 (Status Flag Disable, SFD) should be low.

Pin 25 (Transmitter Register Output, TRO) is the serial data output. Data to be sent is written into the transmit buffer registers via pins 26 to 33 (Transmitter Buffer Registers). When pin 23 (-Transmitter Buffer Register Load,-TBRL) goes low, the data is loaded into the transmitter buffer registers and when it goes from low to high, it

loads the data into the transmitter register and initiates the serial data transmission. Pin 22 is Transmitter Buffer Register Empty. A high level on this indicates that transmitter buffer register has transferred data into the transmitter register and is ready for new data. Pin 24 is Transmitter Register Empty. A high level on this pin indicates the completion of a serial data transmission.

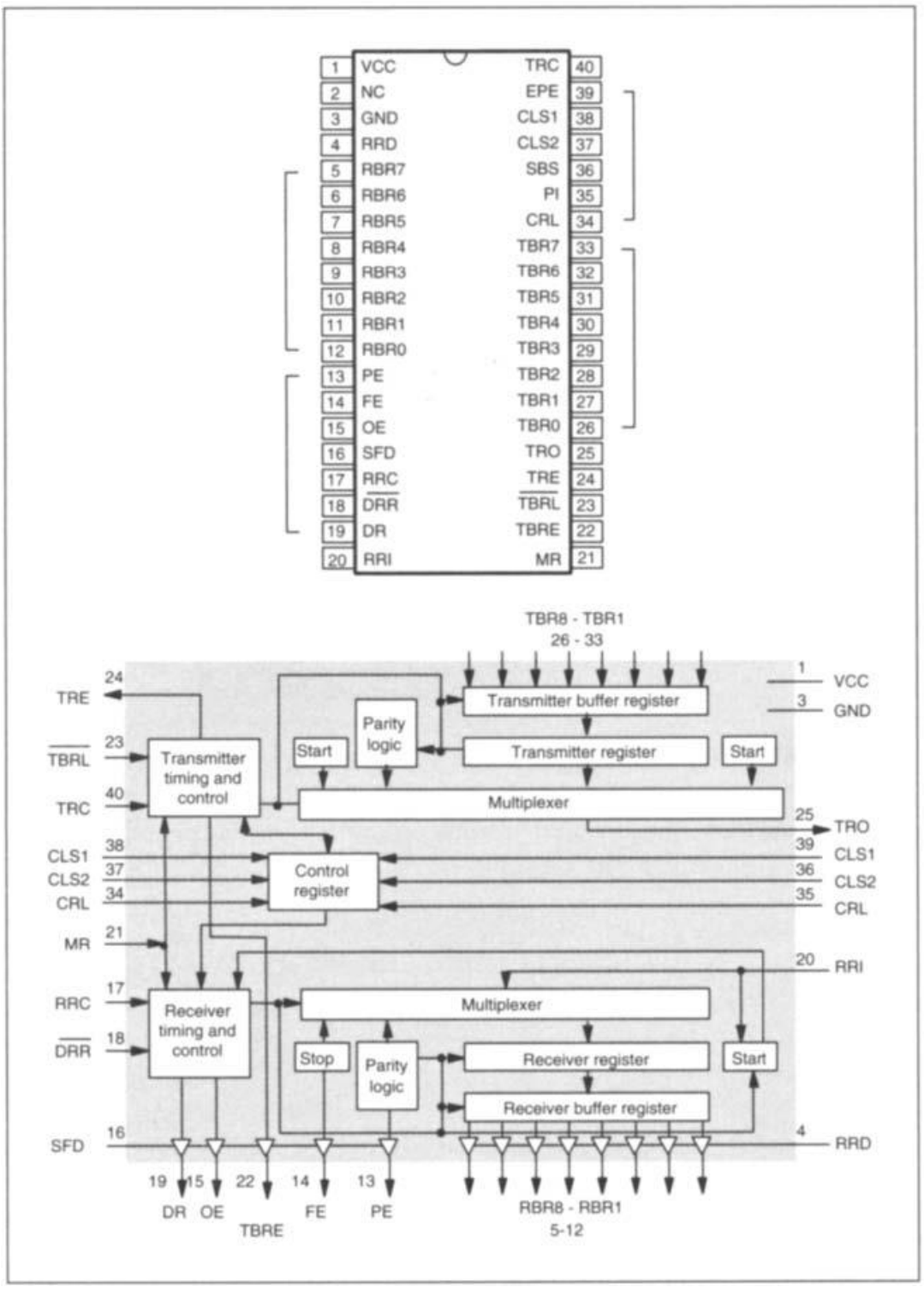


Figure 4.8 Pin-out and internal block diagram of the 6402 UART

An experimental circuit of the 6402 connected to the RS232 experimental board is shown in Figure 4.10. RRI, TRO and -TBRL of the 6402 are connected to TD, RD and DTR terminals on the experimental board. The clock input to the UART is generated by a circuit using a CD4060 and a 2.4576 MHz crystal. From pins 7 of the CD4060, a clock signal at 153.6 kHz is generated, giving a baud rate of 9600. Pin 18 (-DRR) is pulled to logic low. This causes the 6402 to receive serial data continuously.

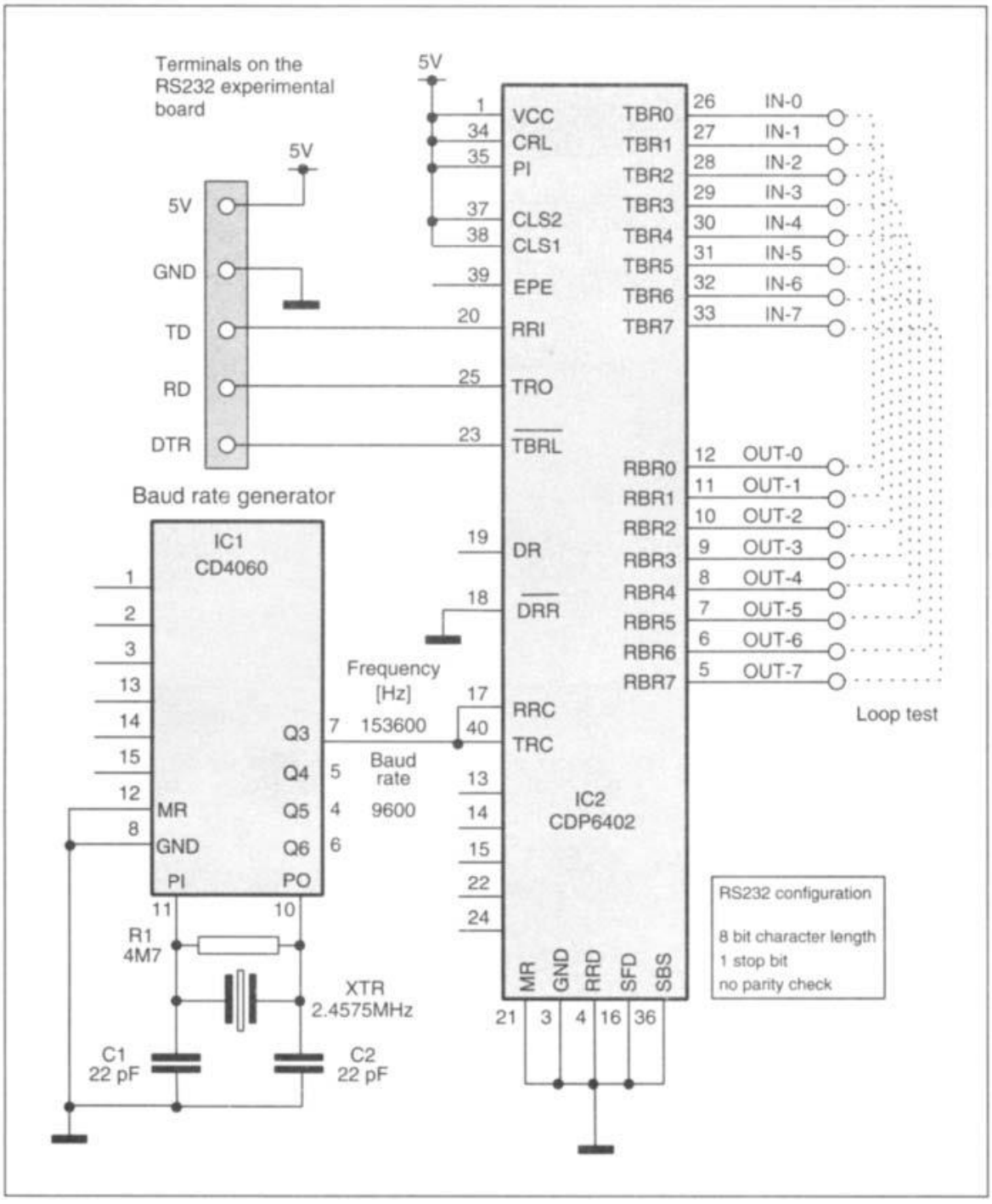


Figure 4.10 Experimental circuit diagram of the 6402 UART

Summary:

1- Liner drivers have a major rule in matching UART and RS232 Voltages.

2- UART Prog chips encapsulate paralle data into serial format without the need for a UC.

Questions:

1- What is a line driver

2- How does the UART Programmable chip works? how is it different from an UC ?